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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,938	04/15/2004	Ludovic Ruat	01RO13054507	7278

27975 7590 12/31/2007

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EXAMINER	
KANGARLOO, RAMTIN	
ART UNIT	PAPER NUMBER
4177	

NOTIFICATION DATE	DELIVERY MODE
12/31/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

creganoa@addmg.com

Office Action Summary	Application No.	Applicant(s)	
	10/824,938	RUAT ET AL.	
	Examiner	Art Unit	
	RAMTIN KANGARLOO	4177	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/15/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/15/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Rakib et al. (US Patent Application Publication No.2001/0024474).

Regarding **Claim 1**, Rakib discloses an asynchronous frame receiver comprising: an input for receiving an asynchronous frame comprising a break character, the break character comprising a plurality of bits having a same value; and a hot-plugging circuit for connecting to an asynchronous data bus that is operating, said hot-plugging circuit detecting the break character, and leaving an initial idle state and switching to at least one operating mode when the break character has been detected (See Page. 21, Paragraph [0241] and Page. 39, Paragraph [0384] and Page. 49, Paragraph [0443]).

Regarding **Claim 2**, Rakib discloses an asynchronous frame receiver according to claim 1, wherein the asynchronous frame further comprises a synchronization character after the break character, the asynchronous frame receiver further comprising: a clock recovery circuit that is activated after receiving the synchronization

character at the input after detecting the break character (See Page. 6, Paragraph [0071] and Page. 46, Paragraph [0429] and Page. 46, Paragraph [0431]).

Regarding **Claim 3**, Rakib discloses an asynchronous frame receiver according to claim 2, wherein said clock recovery circuit measures a clock period in the synchronization character (See Page. 32, Paragraph [0336]).

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Regarding **Claim 4**, Rakib discloses an asynchronous frame receiver according to claim 3, wherein said clock recovery circuit measures a clock period from a first falling edge after the break character to a last falling edge of the synchronization character (See Page. 35, Paragraph [0355]).

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Regarding **Claim 5**, Rakib discloses an asynchronous frame receiver according to claim 1, wherein said hot-plugging circuit comprises a state machine (See Page. 49, Paragraph [0443]).

Regarding **Claim 6**, Rakib discloses an asynchronous frame receiver according to claim 1, further comprising a substrate; and wherein said hot-plugging circuit is on said substrate so that the asynchronous frame receiver comprises an integrated circuit (See Page. 32, Paragraph [0333]).

Regarding **Claim 7**, Rakib discloses a microcontroller comprising: a universal asynchronous frame receiver transceiver (UART) comprising an input for receiving an asynchronous frame comprising a break character, the break character comprising a plurality of bits having a same value; and a hot-plugging circuit for connecting to an asynchronous data bus that is operating, said hot-plugging circuit detecting the break character, and leaving an initial idle state and switching to at least one operating mode when the break character has been detected; and a processor connected to said asynchronous frame receiver (See Page. 21, Paragraph [0241] and Page. 39, Paragraph [0384] and Page. 49, Paragraph [0443] and Fig. 8).

Regarding **Claim 8**, Rakib discloses a microcontroller according to claim 7, further comprising a memory connected to said processor (See Page. 16, Paragraph [0208]).

Regarding **Claim 9**, Rakib discloses a microcontroller according to claim 7, wherein the asynchronous frame further comprises a synchronization character after the break character, said UART further comprising: a clock recovery circuit that is activated after receiving the synchronization character at the input after detecting the break character (See Page. 6, Paragraph [0071] and Page. 46, Paragraph [0429] and Page. 46, Paragraph [0431]).

Regarding **Claim 10**, Rakib discloses a microcontroller according to claim 9, wherein said clock recovery circuit measures a clock period in the synchronization character (See Page. 32, Paragraph [0336]).

Regarding **Claim 11**, Rakib discloses a microcontroller according to claim 10, wherein said clock recovery circuit measures a clock period from a first falling edge after the break character to a last falling edge of the synchronization character (See Page. 35, Paragraph [0355]).

Regarding **Claim 12**, Rakib discloses a microcontroller according to claim 7, wherein said hot-plugging circuit comprises a state machine (See Page. 49, Paragraph [0443]).

Regarding **Claim 13**, Rakib discloses a method for connecting an asynchronous frame receiver to an asynchronous data bus that is operating, the method comprising: setting the asynchronous frame receiver to an initial idle state; receiving at an input of the asynchronous frame receiver an asynchronous frame comprising a break character, the break character comprising a plurality of bits having a same value; and detecting the break character and switching the asynchronous frame receiver from the initial idle state to at least one operating mode (See Page. 21, Paragraph [0241] and Page. 39, Paragraph [0384] and Page. 49, Paragraph [0443]).

Regarding **Claim 14**, Rakib discloses a method according to claim 13, wherein the at least one operating mode comprises a read mode (See Page. 4, Paragraph [0025]).

Regarding **Claim 15**, Rakib discloses a method according to claim 13, wherein the asynchronous frame further comprises a synchronization character after the break character; and further comprising activating a clock recovery circuit after receiving the synchronization character at the input after detecting the break character (See Page. 6, Paragraph [0071] and Page. 46, Paragraph [0429] and Page. 46, Paragraph [0431]).

Regarding **Claim 16**, Rakib discloses a method according to claim 15, wherein the clock recovery circuit measures a clock period in the synchronization character (See Page. 32, Paragraph [0336]).

Regarding **Claim 17**, Rakib discloses a method according to claim 16, wherein the clock recovery circuit measures a clock period from a first falling edge after the break character to a last falling edge of the synchronization character (See Page. 35, Paragraph [0355]).

Conclusion

3. Any response to this Office Action should be **faxed** to (571) 273-8300 **or Mailed to :**

Commissioner for Patents,
P.O.Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to RAMTIN KANGARLOO whose telephone number is (571)270-3452. The examiner can normally be reached on Monday to Thursday 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benny Tieu can be reached on (571) 272-7490. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ramtin Kangarloo/
Examiner, Art Unit 4177
December 18, 2007

/Benny Q Tieu/
Supervisory Patent Examiner, Art Unit 4177